SMG16032B LCM SPECIFICATION

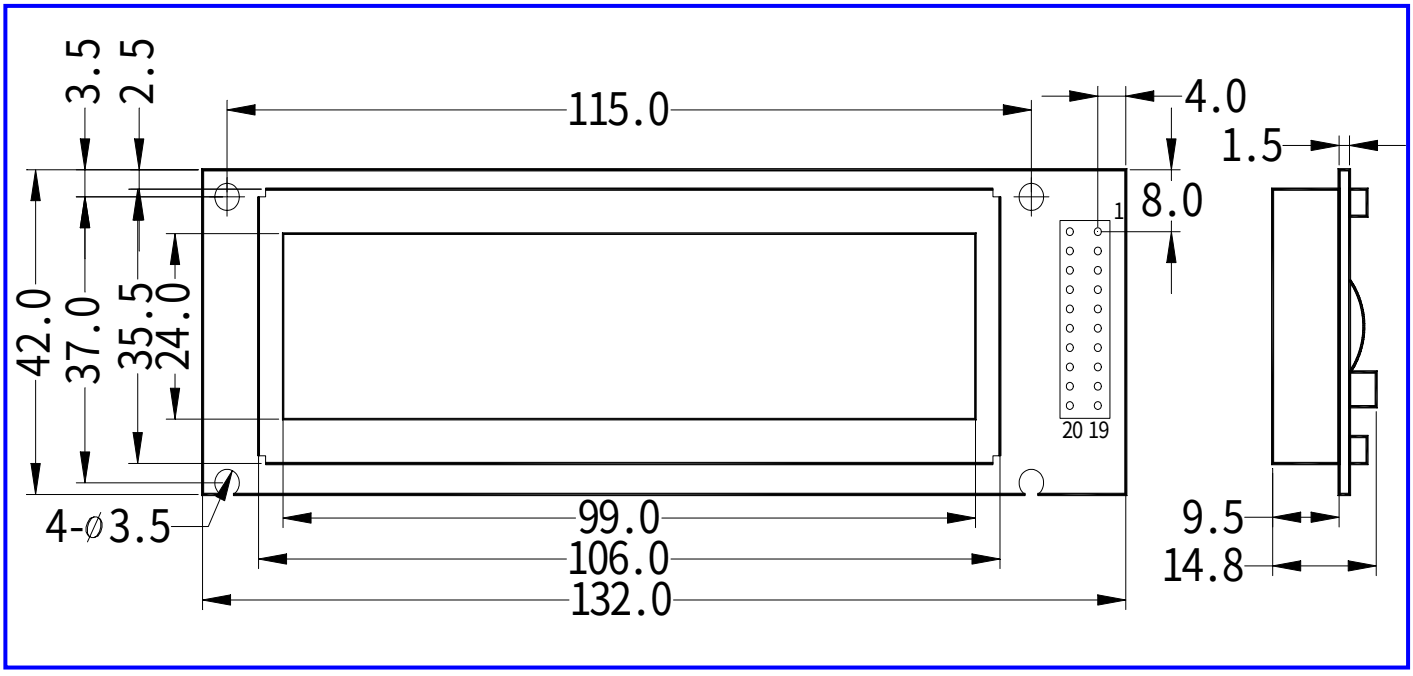
1 MAIN TECHNOLOGY PARAMETER:

Number of dots:	160X32	Color of LCD:	Yellow-Green(STN)
Operating voltage:	4.8~5.2V	Dot size:	0.48X0.48(WXH)mm
Operating current:	220μA(5.0V)	Operating temperature:	0~50℃
Color of LED:	Yellow-Green	Storage temperature:	-20~70℃
Current of LED:	<150mA		

2 PIN DESCRIPTION:

PIN	SYMBOL	SIGNAL DESCRIPTION	PIN	SYMBOL	SIGNAL DESCRIPTION
1	A0	Register select-LOW=Instruction,HIGH=Data	8 to 15	DB0 to DB7	Data BUS-Software selectable 4 or 8 bit mode
2	/CS2	Chip select for IC2	16	RST	Reset the system（H/L）
3	/CS1	Chip select for IC1	17	VEE	Supply Voltage LCD Driver
4	/RD	Read（L）	18	NC	Null
5	/WR	Write（L）	19	BLA	Anode of LED
6	VDD	Power supply（+5V）	20	BLK	Cathode of LED
7	VSS	GND			

3 EXTERNAL DIMENSION:



4 Instruction

The SED1520A distinguish the signal on the data bus by combination of A0 and R/W(/RD,/WR).Normally,the busy check is not required as the SED1520A is operating so first because of the decode of the instruction and execution are performs only depend on the internal timing which not depend on the external clock.

The Table.1 shows the instruction codes of the SED1520A.

Table 1. Instruction Code

Instruction	Code											Description
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
Display On/Off	0	1	0	1	0	1	0	1	1	1	0/1	Whole Display On/Off. 1:On,0:Off(Power Save mode if the static Drive On)
Display Start Line	0	1	0	1	1	0	Display Start Address (1~31)					Determine the Display Line correspond to the COM0.
Page Address Set	0	1	0	1	0	1	1	1	0	Page (0~3)		Set the Page of Disp.Dta RAM to the Page Register.
Column Address Set	0	1	0	0	Column Address (0~79)							Set the Column Address of Display Data RAM to the Column Register.
Status Read	0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0	Read the ststus. BUSY 1:Working,0:Ready ADC 1:Clockwise Output 0:Counterclockwise ON/OFF 1:Disp off 0:Disp ON RESET 1:Reset,0:Normal
Write Display Data	1	1	0	Write Data								Write the data to the Display Data RAM. Access the predetermined address of the Display Data RAM. The Column add-ress increment “1” after read or write.
Read Display Data	1	0	1	Read Data								Read the data from the Display Data RAM
ADC Select	0	1	0	1	0	1	0	0	0	0	0/1	Determine the clockwise or counterclockwise reading of the Display Data RAM. 0:Clockwise Output 1:Counterclockwise Output
Static Drive On/Off	0	1	0	1	0	1	0	0	1	0	0/1	Select the Dynamic or Static Driving. 1:Static Driving (Power

												Saving) 0:Dynamic Driving
Duty Ratio Select	0	1	0	1	0	1	0	1	0	0	0/1	Select the duty ratio. 1:1/32 Duty,0:1/16 Duty
Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the column Address register when writing but no-change when reading.
End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify Write Mode.
Reset	0	1	0	1	1	1	0	0	0	1	0	Set the Display Start Line Register to 1st line,Column Add.Counter and Page Add.Register to “0”.
Power Save (Dual Command)	0 0	1 1	0 0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1	Set the power save mode by selecting Display off and Static Driving On.

5 Explanation of instruction Code

(a) Display On/Off

This instruction executes whole display On/Off no relation with the data in the Display Data RAM and Internal conditions.

	A0	/RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	1	0	1	0	1	0	1	1	1	D

D 0:Display On
1:Display Off

When the static driving mode is selected(static drive On) in display Off status, the internal circuits put on the power save mode.

(b) Display Start Line

This instruction set the line address as shown Fig.1.The selected line in the Display Data RAM correspond to the COM0 which display at the top of LCD panel.

The display area is set automatically from the selected line to the line which increased the number of duty ratio.

Therefore,the smooth scroll for vertical direction by changing the start line address one by one or page switching sre available by this instruction.

	A0	/RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	1	0	1	1	0	A4	A3	A2	A1	A0

A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0
				1	1

1	1	1	1	0	1E
1	1	1	1	1	1F

(c) Page Address Set

When MPU access the Display Data RAM,the page address corresponded to the address must be selected.

The access in the Display Data RAM is available by setting the page and column address.

The display is no change when the page address is changed.

	A0	/RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	1	0	1	0	1	1	1	0	A1	A0

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

(d) Column Address Set

This instruction set the column address in the Display Data RAM.

When the MPU access the Display Data RAM continuously, the column address increase “1” automatically, the MPU can access the data only without address setting.

The increment of the column address is stopped by the address of 4FH automatically, but the page address is no change even if the column address increase to 4FH and stop.

	A0	/RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	1	0	0	A6	A5	A4	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	Column Add.
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
1	0	0	1	1	1	0	4E
1	0	0	1	1	1	1	4F

(e) Status Read

This instruction read out internal status.

	A0	/RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 Indicate the operating or Reset cycle.
The instruction can input after the BUSY status change to “0”.

ADC : Indicate the output correspondence of column(segment)address and segment driver.
0:Counterclockwise output(Inverse)column Address 79-n ←→Segment Driver n
1:Clockwise Output (normal) column Address n ←→Segment Driver n

ON/OFF: Indication the whole display On/Off status.
0:Whole Display “On”

1:Whole Display “Off”

(Note) The data “0=On” and “1=Off” of Display On/Off status read out is inverted with the Display On/Off instruction data of “1=On” and “0=Off”.

RESET : Indicate the initialization period by /RST signal or reset instruction.

(f) Write Display Data

This instruction write the 8-bit data on the data bus into the Display Data RAM.

The column(segment) address increase “1” automatically when writing, the MPU can write the 8-bit data into the Display Data RAM without address setting.

	A0	/RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
Code	1	1	0	Write Data							

(g) Read Display Data

This instruction read out the 8-bit data from Display Data RAM which address by the column and page address. In case of the read Modify Write Mode if Off, the column address increase “1” automatically after each read out, therefore, the MPU Can read out the 8-bit data from the Display Data RAM continuously without address setting.

One time of dummy read must be required after column address set as explain in (6-3).

	A0	/RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
Code	1	0	1	Read Data							

(h) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver output. Therefore, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.

	A0	/RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	1	0	1	0	1	0	0	0	0	D

D 0:Clockwise Output (Inverse)
1:CounterClockwise Output (Normal)

(i)Static Drive On/Off

This instruction executes the all common output turns on and whole display on obligatory.

	A0	/RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	1	0	1	0	1	0	0	1	0	D

D 0:Static Drive Off (Normal Operation)
1:Static Drive On (Whole Display Turns On)

When the Display Off mode is selected(Display Off) in Static Drive On status, the internal circuits put on the power save mode.

(j) Duty Select

This instruction set the LCD Driving duty ratio.

	A0	/RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	1	0	1	0	1	0	1	0	0	D

D 0:1/16 duty
1:1/32 duty

(k) Read Modify Write

After this instruction is executed, the column address increase “1” automatically when Display Data Write Instruction execution, but the address is not changed when the Display Data Read Instruction execution.

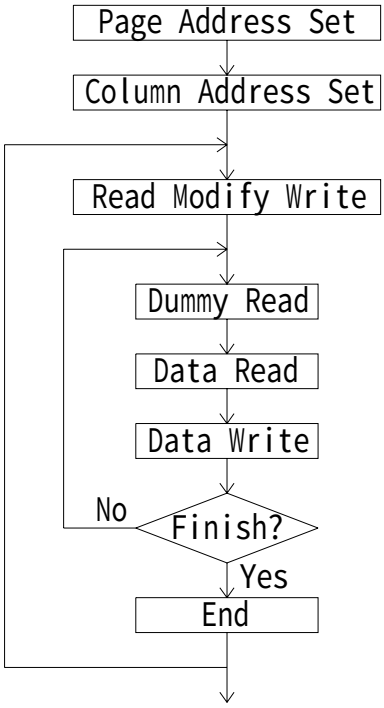
This status continues during End instruction execution. When the End instruction is entered the column address back to the address where Read Modify instruction entering.

By this function, the load of MPU for example cyclic data writing operation like as cursor blink ect., can be reduced.

			R/W								
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	1	0	1	1	1	0	0	0	0	0

(Note) During the Read Modify Write mode, any instruction except Column Address Set can be executed.

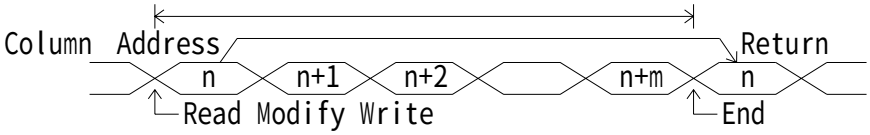
(l) Sequence of cursor display



(m) End

This instruction release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

			R/W								
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	1	0	1	1	1	0	1	1	1	0



(n) Reset

This instruction executes the following initialization.

Initialization

① Set the 1st line in the Display Start Line Register.

② Set the page 3 in the Page Register.

In this time, there are no influence to the Display Data RAM.

	A0	/RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	1	0	1	1	1	0	0	0	1	0

The reset signal input to the /RST terminal must be required for the initialization when the power turns on.

(Note) The initialization when the power turns on can not be executed by Reset instruction.

(o) Power Save (Dual Command)

When both of Display Off and Static Drive On are executed, the internal circuits put on the power save mode and the current consumption is reduced as same as stand by current.

The internal status in this mode are as follows;

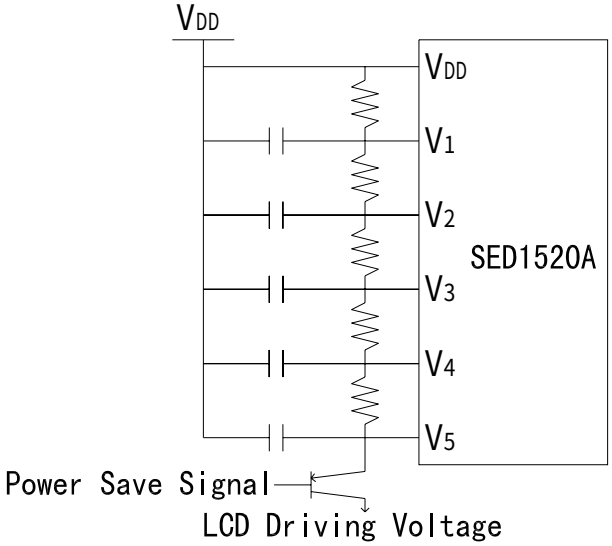
① Stop the LCD Driving. Segment and Common drivers output V_{DD} level.

② Stop the oscillation or the external clock input. Then the terminal OSC_2 becomes floating status.

③ Keeping the display data and operating mode.

The power save mode is released by Display on or static drive off instruction.

To reduce the total power consumption, the current flow on the bleeder resistance must be cut by the transistor etc. during the power save mode as shown below.



6 MPU Interface

(6-1) 68 or 80 type MPU interface selection.

The SED1520A can interface both of 68 or 80 type MPU bus directly by the /RST level after reset instruction entered as shown Table.2.

The data transfer is executed between D0~D7 of SED1520A and the MPU data bus.

During the CS signal is “H”, the SED1520A released from the MPU and becomes stand-by mode.

But the reset instruction can be input though the internal status of SED1520A.

Table.2.

Level of /RST	Type of MPU	A0	E	R/W	D0~D7
“L”	68 type	↑	↑	↑	↑
“H”	80 type	↑	/RD	/WR	↑

(6-2) Discrimination of the data bus signal.

The SED1520A discriminates the data bus signal by combination of A0,E(/RD),and R/W(/WR) signals as shown Table.3.

Table.3.

Common	68 type	80 type		Function
A0	R/W	/RD	/WR	
1	1	0	1	Display Data Read out
1	0	1	0	Display Data Write
0	1	0	1	Status Read
0	0	1	0	Command Input to the Register

(6-3) Access to the Display Data RAM and Internal Regiater.

The SED1520A is operating as one of Pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when the MPU write the data into the display Data RAM, the data is held in the bus-holder at once then write into the Display Data RAM by next data write cycle.

Therefore high speed data transmission between MPU and SED1520A is available because of the limitation of access time of SED1520A locking from MPU is just determined by the cycle time only which ignored the access time of t_{ACC} and t_{DS} of Display Data RAM.

If the cycle time can not be kept in the MPU operation, NOP operation cycle must be insert which equivalent to the waiting operation.

Please note that the read out data is a address data when the read out execution just after the address setting. Therefore, one dummy read is required after address setting or write cycle as shown in Fig.1.

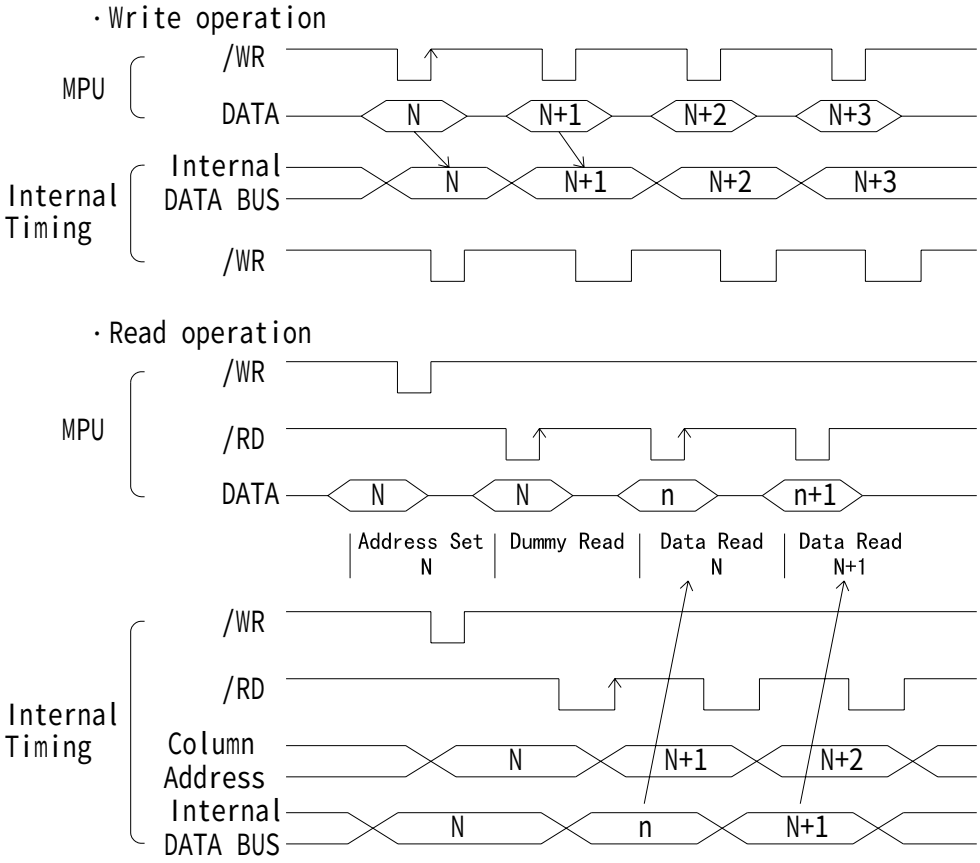


Fig.1 MPU Interface Timing

7 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage(1)	V_{DD}	-0.3~+7.0	V
Supply Voltage(2)	V_1~V_5(3)	V_{DD}-13.5~V_{DD}+0.3	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Operating Temperature	T_{opr}	-30~+80	℃
Storage Temperature	T_{stg}	-55~-125	℃

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{ss}=0V.

Note 3) The relation : $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must be maintained.

8 ELECTRICAL CHARACTERISTICS

(V_{DD}=5V±10%,V_{ss}=0V,Ta=-20~75℃)

PARAMETER		SYMBOL	CONDITION		MIN	TYP	MAX	UNIT	Note
Operating Voltage(1)	Recommend	V_{DD}			4.5	5.0	5.5	V	
	Available				2.4		6.0		4
Operating Voltage(2)	Recommend	V_5			V_{DD}-13.5		V_{DD}-3.5	V	
	Available				V_{DD}-13.5				
	Available	V_2	V_{LCD}=V_{DD}-V_5		V_{DD}-0.6XV_{LCD}				
	Available	V_3			V_5		V_{DD}-0.4XV_{LCD}		
Input Voltage	1	V_{IHT}	CS,A0,D_0~D_7,E,R/W Terminals		2.0		V_{DD}	V	
		V_{ILT}			VSS		0.8		
	2	V_{IHC}	CL,FR,/RST Terminals		0.8XV_{DD}		V_{DD}		
		V_{ILC}			V_{SS}		0.2XV_{DD}		
Output Voltage		V_{OHT}	D0~D7 Terminals	IOH=3.0mA	2.4			V	
		V_{OLT}		IOL=3.0mA			0.4		
	1	V_{OHC1}	FR Terminal	I_{OH}=-2.0mA	2.4				
		V_{OLC1}		I_{OL}=2.0mA			0.4		
Input Leakage Current		I_{LI}	A0,E,R/W,CS,CL,/RST		-1.0		1.0	μA	
		I_{LO}	D_0~D_7,FR Terminals		-3.0		3.0		5
Driver On-risistance		R_{ON}	Ta=25℃	V5=V_{DD}-5.0V		5.0	7.5	KΩ	6
				V5=V_{DD}-3.5V					
Stand-by Current		I_{DDQ}	CS=CL=VDD			0.05	1.0	μA	
Operating Current		I_{DD1}	Display V_5=V_{DD}-5.0V f_{CL}=2kHz			2.0	5.0	μA	
		I_{DD2}	Accessing,tcyc=200kHz			300	500		7

Reset time	tr	/RST Terminal	1.0		1000	μs	

Note 4) SED1520A can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 5) Apply to the High-impedance state of D0 to D7 and FR terminals.

Note 6) R_{ON} is the resistance values between power supply terminals(V_1,V_2,V_3,V_4) and each output terminals of common and segment supplied by 0.1V.

Note 7) The IDD2 is specified under the condition of cyclic(tcyc) inverted data input continuously.
The operating current during the accessing is proportionate to the frequency of tcyc.
In the no accessing it is as same as IDD1.

9 BUS TIMING CHARACTERISTICS

・Read/Write operation sequence(68 Type MPU)

(V_{DD}=5V±10%,V_{ss}=0V,Ta=-20~75℃)

P A R M E T E R			SYMBOL	MIN	MAX	CONDITION	NIT
Address Set Up Time		A0,R/W Terminals	t_{AW6}	20			ns
Address Hold Time			t_{AH6}	10			
System Cycle Time			t_{CYC6}	1000			
Enable Pulse Width	Read	E Terminals	t_{EW}	100			
	Write			80			
Data Set Up Time		D_0~D_7 Terminals	t_{DS6}	80			
Data Hold Time			t_{DH6}	10			
Access Time			t_{ACC6}		90	C_L=100pF	
Output Disable Time			t_{CH6}	10	60		

Note 8) Input signal rise time(t_r) and flal time(t_f) are less than 15ns.

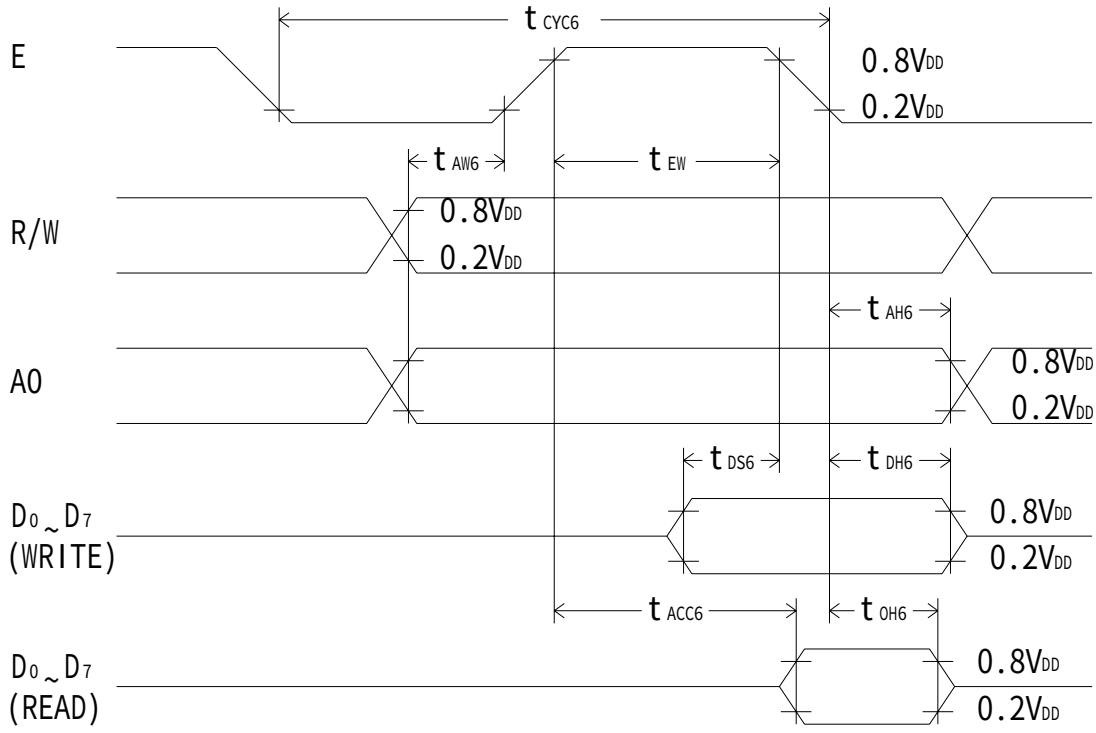


Fig.2 Bus Read/Write operation sequence(68 Type MPU)

· Read/Write operation sequence(80 Type MPU)

(V_{DD}=5V±10%,V_{ss}=0V,Ta=-20~75℃)

P A R M E T E R		SYMBOL	MIN	MAX	CONDITION	NIT
Address Set Up Time	A0,R/W	t_{AW8}	20			ns
Address Hold Time	Terminals	t_{AH8}	10			
System Cycle Time	/RW,/WR	t_{CYC8}	1000			
Control Pulse Width	Terminals	T_{CC}	200			
Data Set Up Time		t_{DS8}	80			
Data Hold Time	D_0~D_7	t_{DH8}	10			
RD Access Time	Terminals	t_{ACC8}		90	C_L=100pF	
Output Disable Time		t_{CH8}	10	60		

Note 9) Input signal rise time(t_r) and fall time(t_f) are less than 15ns.

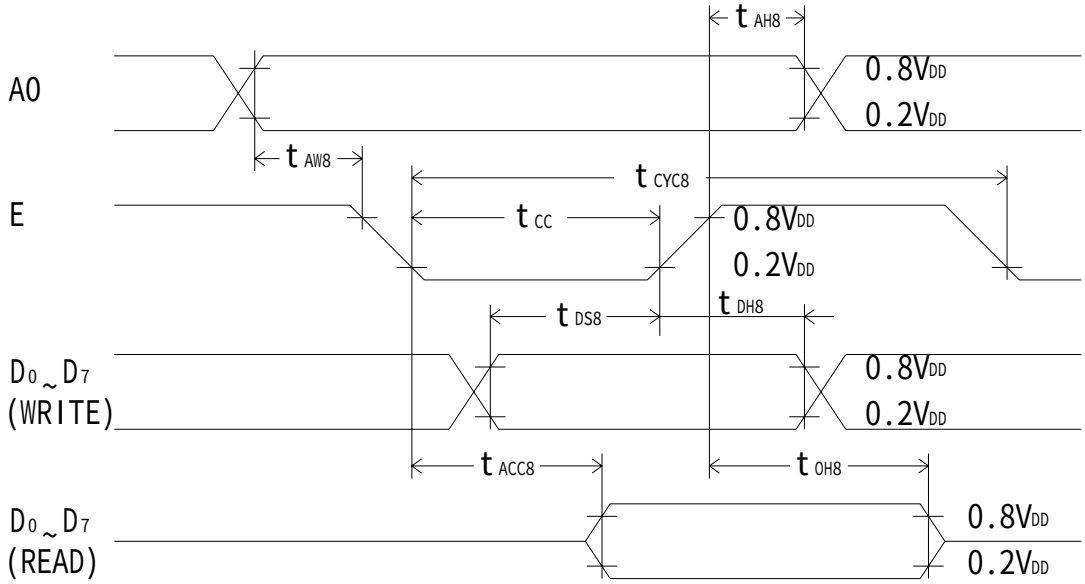


Fig.3 Bus Read/Write operation sequence(80 Type MPU)

· Display control timing characteristics(Both of 68 and 80 type MPU)

Input Timing (V_{DD}=5V±10%,V_{ss}=0V,Ta=-20~75℃)

P A R A M E T E R	SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
“L” level Pulse Width	t_{WLCL}	35				μs
“H” level Pulse Width	t_{WHCL}	35				
Rise Time	t_r		30	150		ns
Fall Time	t_f		30	150		
FR Delay Time(SED1520A Slave)	t_{DFR}	-2.0		2.0		μs

Input Timing

P A R A M E T E R	SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
FR Delay Time(SED1520A Master)	T_{DFR}		0.2	0.4	C_L=100pF	μs

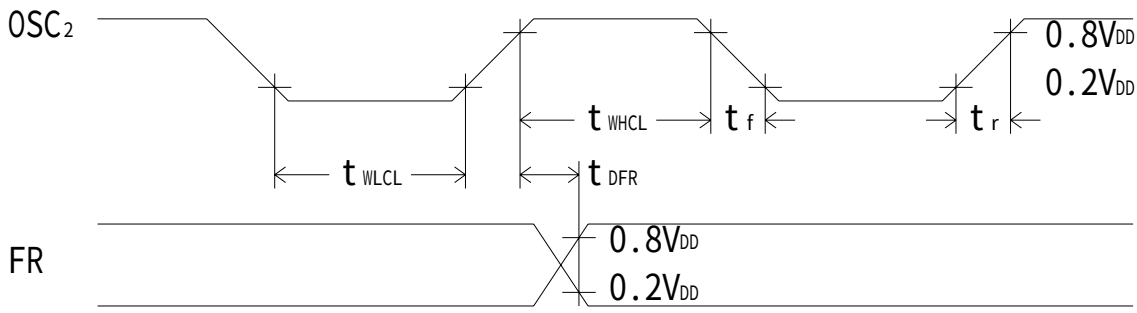


Fig.4 Display control timing characteristics

10 REFERENCE WEBPAGE: http://www.sunman.com.cn/lcm/product/SMG16032B.html