SMG12864D LCM SPECIFICATION

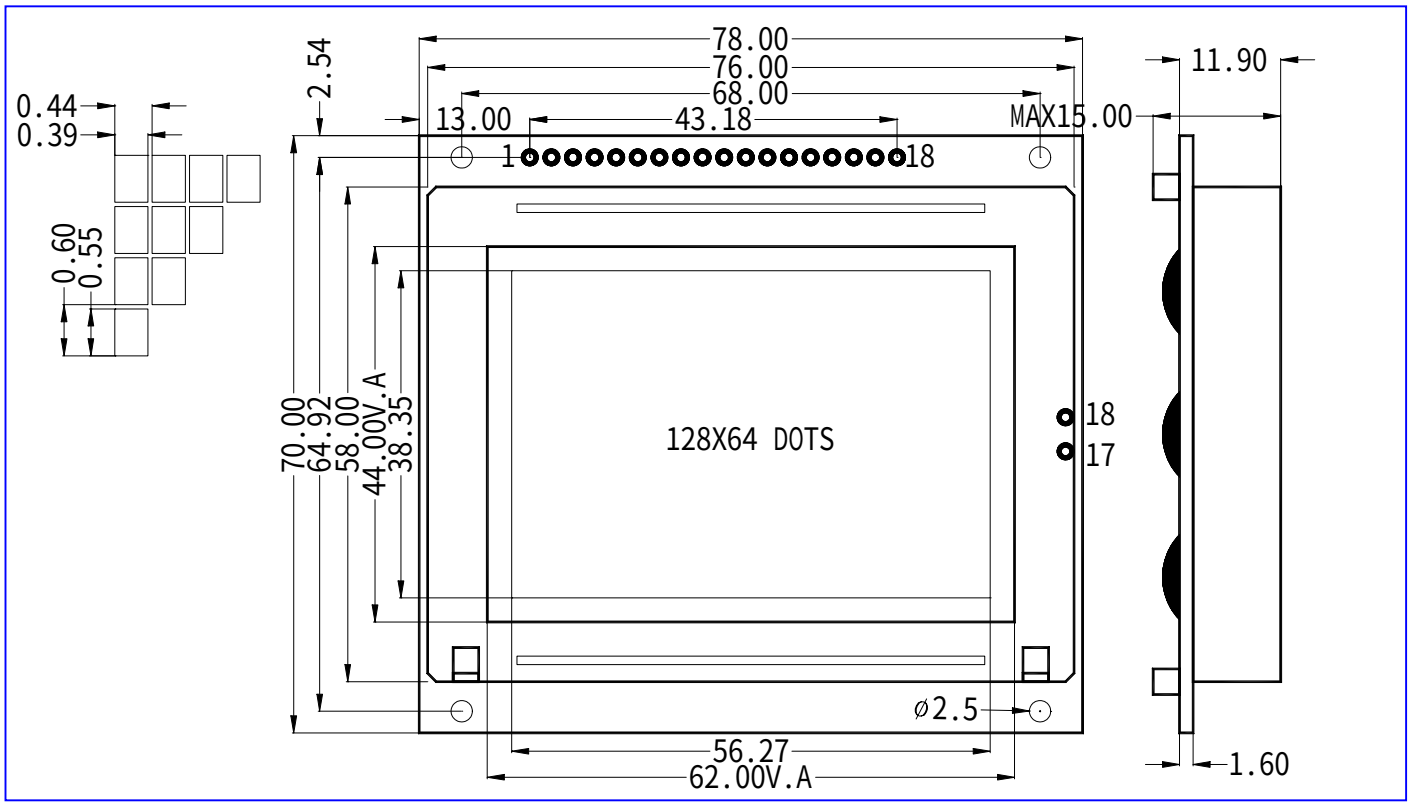
1. MAIN TECHNOLOGY PARAMETER:

Number of dots:	128X64	Color of LCD:	Yellow-Green（STN）
Operating voltage:	4.8~5.2V	Dot size:	0.39X0.55(WXH)mm
Operating current:	4.0mA(5.0V)	Operating temperature:	
Current of LED:	80.0mA	Storage temperature:	

2. PIN OCNFIGURATION:

PIN	SYMBOL	SIGNAL DESCRIPTION	PIN	SYMBOL	SIGNAL DESCRIPTION
1	CS2	Chip select for IC2	7	R/W	Read/Write LOW=MPU to LCM,HIGH=LCM to MPU
2	CS1	Chip select for IC1	8	E	Enable,R/W=LOW:Data are talking over at falling edge; R/W=HIGH:Data can be read at E=1
3	VSS	GND	9 to 16	DB0 to DB7	Data BUS-Software selectable 4 or 8 bit mode
4	VDD	Power Supply （+5V）	17	BLA	Anode of LED
5	NC	Null	18	BLK	Cathode of LED
6	RS	Register select- LOW=Instruction,HIGH=Data			

3. EXTERNAL DIMENSION:



4. ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD}=+5V±10%,V_{SS}=0V,V_{DD}-V_{EE}=8~17V,Ta=-30~85oC)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit	Note
Input High Voltage	V_{IH1}	-	0.7V_{DD}	-	V_{DD}	V	*1
	V_{IH2}	-	2.0	-	V_{DD}	V	*2
Input Low Voltage	V_{IL1}	-	0	-	0.3V_{DD}	V	*1
	V_{IL2}	-	0	-	0.8	V	*2
Output High Voltage	V_{OH}	I_{OH}=200μA	2.4	-	-	V	*3
Output Low Voltage	V_{OL}	I_{OL}=1.6mA	-	-	0.4	V	*3
Input Leakage Current	I_{LKG}	V_{IN}=V_{SS}~V_{DD}	-1.0	-	1.0	μA	*4
Three-state(OFF) Input Current	I_{TSL}	V_{IN}=V_{SS}~V_{DD}	-5.0	-	5.0	μA	*5
Driver Input Leakage Current	I_{DIL}	V_{IN}=V_{EE}~V_{DD}	-2.0	-	2.0	μA	*6
Operating Current	I_{DD1}	During Display	-	-	100	μA	*7
	I_{DD2}	During Access Access Cycle=1MHz	-	-	500	μA	*7
On Resistance	R_{ON}		-	-	7.5	KΩ	*8

*1.CL,FRM,M,RSTB,CLK1,CLK2
*2.CS1B,CS2B,XS3,E,R/W,RS,DB0~DB7
*3. DB0~DB7
*4.Except DB0~DB7
*5.DB0~DB7 at High Impedance
*6.VOL(R),V2L(R),V3L(R),V5L(R)
*7.1/64 duty, FCLK=250KHz, Frame Frequency=70Hz, Output:No Load
*8.V_{DD}~V_{EE}=15.5V
VOL(R)>V2L(R)=V_{DD}-2/7(V_{DD}-V_{EE})>V3L(R)=V_{EE}+2/7(V_{DD}-V_{EE})>V5L(R)

AC Characteristic (V_{DD}=+5V±10%,V_{SS}=0V,V_{DD}-V_{EE}=8~17V,Ta=-30~85oC)

MPU Interface

Characteristics	Symbol	Min	Typ	Max	Unit
E Cycle	t_C	1000	-	-	ns
E High Level Width	t_{WH}	450	-	-	ns
E Low Level Width	t_{WL}	450	-	-	ns
E Rise Time	t_R	-	-	25	ns
E Fall Time	t_F	-	-	25	ns
Address Set-Up Time	t_{ASU}	140	-	-	ns
Address Hold Time	t_{AH}	10	-	-	ns
Data Set-Up Time	t_{DSU}	200	-	-	ns
Data Delay Time	t_D	-	-	320	ns
Data Hold Time(Write)	t_{DHW}	10	-	-	ns
Data Hold Time(Read)	t_{DHR}	20	-	-	ns

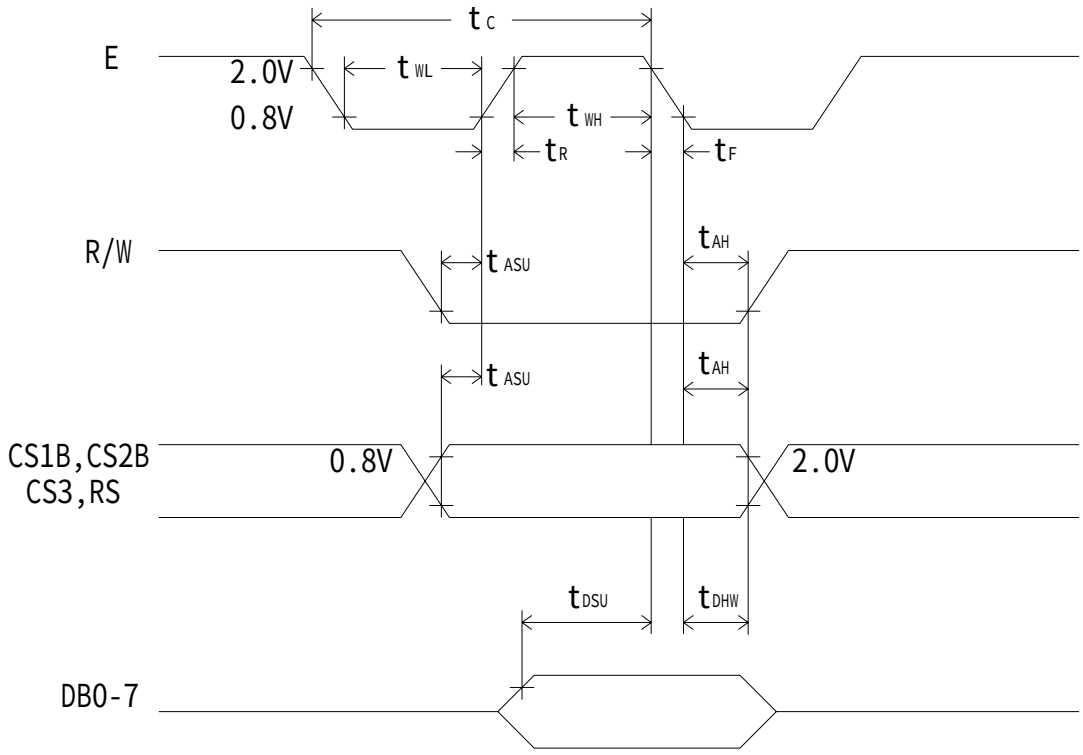


Fig 1.MPU write timing

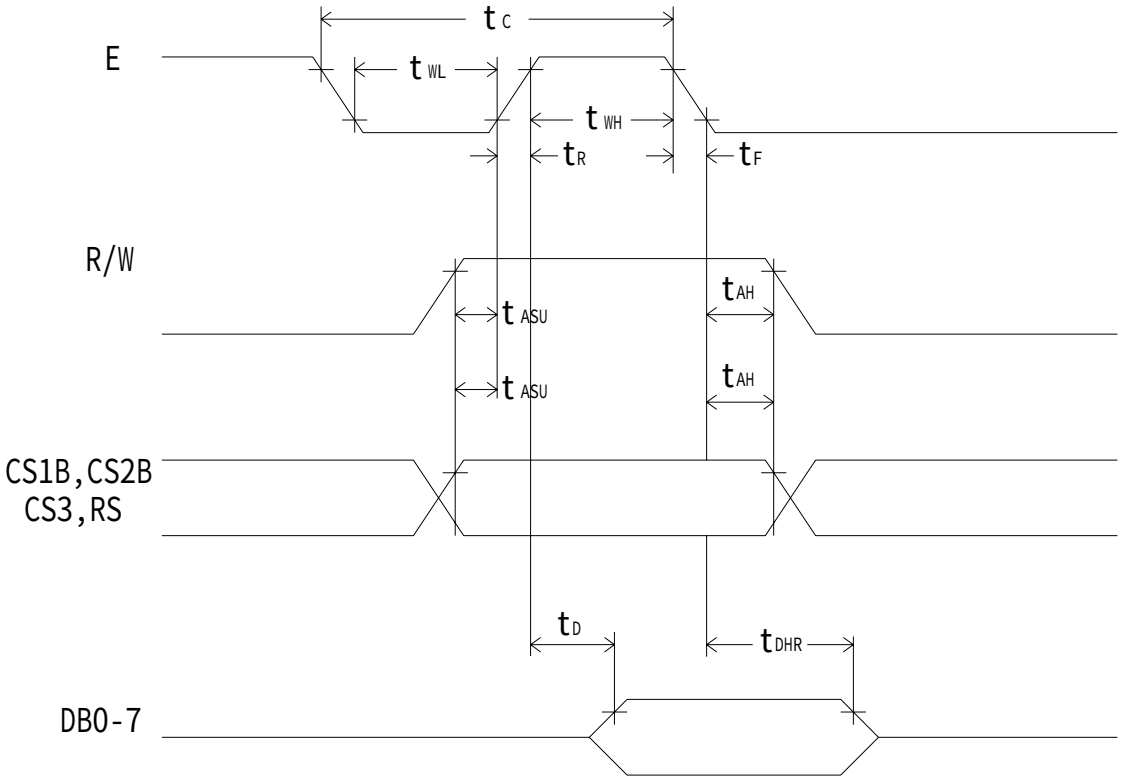


Fig 2.MPU write timing

5. OPERATING PRINCHIPLES & METHODS

1.I/O Buffer

Input buffer control the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction dose not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS1B~CS3.

2.Input register

Input register is provided to interface with MPU witch is different operating frequency. Input register stores the data temporarily before writing it into display RAM.

When CS1B to CS3 are in the active mode, R/W and R/S select the input register. The data from MPU is written into input register. Then Writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

3.Output register

Output register stores the data temporarily from display data RAM when CS1B,CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H,RS=L, status data(busy check) can read out.

To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read, But status read is not needed dummy read.

RS	R/W	Function
L	L	Instruction
	H	Status read(busy check)
H	L	Data write(from input register to display data RAM)
	H	Data read(From display data RAM to output register)

4.Reset

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU. When RSTB becomes low, following procedure is occurred.

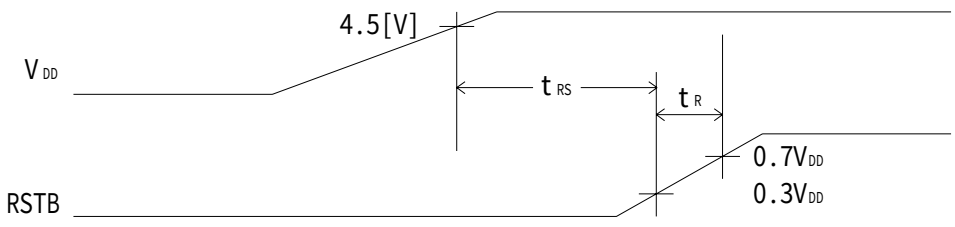
1) Display off
2) Display start line register become set by 0(Z-address 0)

While RSTB is low, No instruction except status read can be accepted. Therefore, execute other instruction after making sure that DB4=0(clear RSTB) and DB7=0(ready) by status read instruction.

The Conditions of power supply at initial power up are shown in table 1.

Table 1.Power Supply Initial Condition

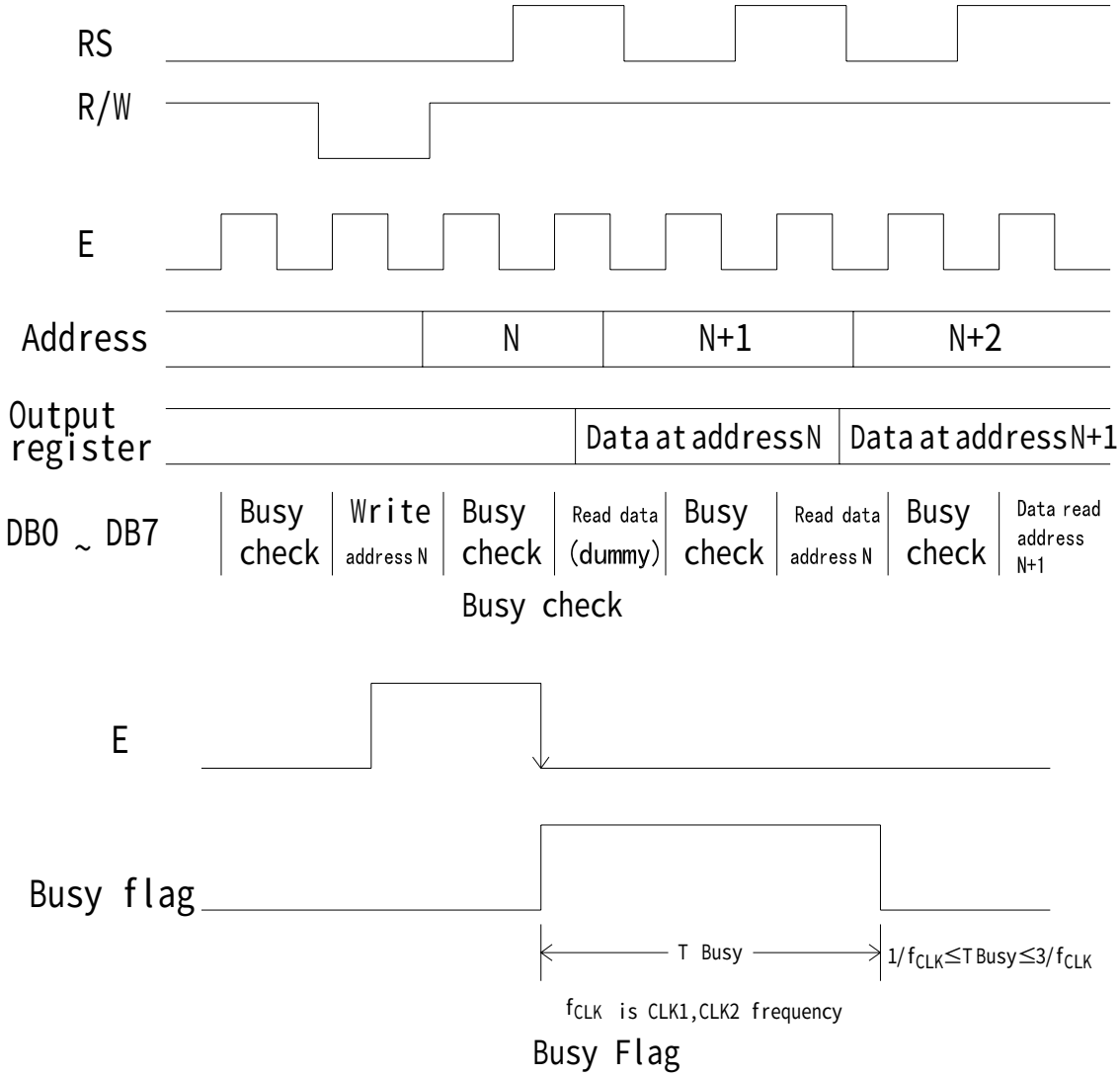
Item	System	Min	Typ	Max	Unit
Reset Time	T_{RS}	1.0	-	-	μs
Rise Time	t_R	-	-	200	μs



5.Busy flag

Busy flag indicates that KS0108B is operating or no operating. When busy flag is high, KS0108B is in internal operating. When busy flag is low, KS0108B can accept the data or instruction.

DB7 indicates busy flag of the KS0108B.



Busy Flag

6.Display On/Off flip-Flop

The display on/off flip makes on/off the liquid crystal display. When flip-flop is reset(logical low), selective voltage or non selective voltage appears on segment output terminal. When flip-flop is set(logic high), non selective voltage appears on segment output terminal regardless of display RAM data.

The display on/off flip-flop can changes status by instruction. The display data at all segment disappear while RSTB is low.

The status of the flip-flop is output to DB5 by status read instruction.

The display on/off flip-flop synchronized by CL signal.

7.X Page Register

X page register designates pages of the internal display data RAM.

Count function is not available. An address is set by instruction.

8.Y address Counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

9.Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display, write data 1. The other way, off state, writes 0.

Display data RAM address and segment output can be controlled by ADC signal.

ADC=H=>Y-address 0:S1~Yaddress 63:S64

ADC=L=>Y-address 0:S64~Yaddress 63:S1

ADC terminal connect the V_{DD} or V_{SS}.

10.Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display.

Bit data(DB<0:5>) of the display start line set instruction is latched in display start line register.

Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter.

It is used for scrolling of the liquid crystal display screen.

5. DISPLAY CONTROL INSTRUCTION

The display control instruction control the internal state of the KS0108B. Instruction is received from MPU to KS0108B for the display control. The following table shows various instruction.

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display ON/OFF	L	L	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L:OFF,H:ON
Set Address (Y address)	L	L	L	H	Y Address(0~63)						Sets the Y address in the Y address counter
Set Page (X address)	L	L	H	L	H	H	H	Page(0~7)			Sets the X address at the X address register
Display start line (Z address)	L	L	H	H	Display start line(0~63)						Indicates the display data RAM display at the top of the screen
Status Read	L	H	BUSY	L	ON/OFF	RESET	L	L	L	L	Read status. BUSY L: Ready H: In operation ON/OFF L: Display ON H: Display OFF RESET L: Normal H: Reset

Write Display Data	H	L	Write Data	Write data(DB0:7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read Display Data	H	H	Read Data	Reads data(DB0:7) from display data RAM to the data bus.

1. Display On/Off

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

The display data appears when D is 1 and disappears when D is 0.
Though the data is not on the screen with D=0, it remains in the display data RAM.
Therefore, you can make it appear by changing D=0 into D=1.

2. Set Address(Y Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Y address(AC0~AC5) of the display data RAM is set in the Y address counter.
An address is set by instruction and increased by 1 automatically by read or write operations.

3. Set Page(X Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

X address(AC2~AC0) of the display data RAM is set in the X address register.
Writing or reading to or from MPU is executed in this specified page unit the next page is set.

4. Display Start Line(Z Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

Z address(AC5~AC0) of the display data RAM is set in the display start line register and displayed at the top of the screen.
When the display duty cycle is 1/64 or others(1/32~1/64), the data of total line number of LCD screen from the line specified by display start line instruction is displayed.

5. Status Read

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	BUSY	0	ON/OFF	RESET	0	0	0	0

- BUSY
  When BUSY is 1, the Chip is executing internal operation and no instructions are accepted,
  When BUSY is 0,the Chip is ready to accept any instructions.
- ON/OFF
  When ON/OFF is 1, the display is on.

When ON/OFF is 0, the display is off.

- RESET

When RESET is 1, the system is being initialized.

In this condition, no instructions except status read can be accepted.

When RESET is 0, initializing has finished and the system is in the usual operation condition.

6. Write Display Data

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	D7	D6	D5	D4	D3	D2	D1	D0

Writes data(D0~D7)into the display data RAM.

After writing instruction, Y address is increased by 1 automatically.

7. Read Display Data

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Reads data(D0~D7) from the display data RAM.

After reading instruction, Y address is increased by 1 automatically.

7. REFERENCE WEBPAGE: http://www.sunman.com.cn/lcm/product/SMG12864D.html